IN THE SPECIFICATION:

Please replace the paragraph beginning on Page 1, line 9, with the following:

An FED panel with a conventional FED is illustrated in FIG. 1. A cathode 2 is formed over a substrate 1 with a metal such as chromium (Cr), and a resistor layer 3 is formed over the cathode 2 with an amorphous silicon. A gate insulation layer 4 with a well 4a, through which the bottom of the resistor layer 3 is exposed, is formed on the resistor layer 3 with an insulation material such as SiO_2. A micro-tip 5 formed of a metal such as molybdenum (Mo) is located in the well 4a. A gate electrode 6 with a gate 6a aligned with the well 4a is formed on the gate insulation layer 4. An anode 7 is located a predetermined distance above the gate electrode 6. The gate electrode 7 is formed on the inner surface of a faceplate 98 that forms a vacuum cavity in associated with the substrate 1. The faceplate 8 and the substrate 1 are spaced apart from each other by a spacer (not shown), and sealed at the edges. As for color displays, a phosphor screen (not shown) is placed on or near the anode 7.

Please replace the paragraph bridging Pages 1 and 2 with the following:

The conventional FED emits a small amount of electrons from the micro-tip, so that a high gate voltage is required for high emission current densities. However, if the gate voltage level is beyond a predetermined voltage limit, the problems of leakage current and short life time occur. For these reasons, increasing the gate voltage is limited. As an experiment result, the frequency of arcing increases with higher gate voltage level. When an arcing occurs in the FED, damage caused by the arcing is detected at the edges of the

gate 6a of the gate electrode 6, wherein the gate ~~61~~ 6a serves as a passageway of electrons. Also, an electrical short occurs between the anode 7 and the gate electrode ~~76~~ 6 due to the arcing. As a result, a high anode voltage is applied to the gate electrode 6, thereby damaging the gate insulation layer 4 below the gate electrode 6, and the resistor layer 3 exposed through the well 4a. This damage is more likely caused as the gate and anode voltage levels increase.

Please replace the paragraph beginning on Page 2, line 14, with the following:

It is preferable that a resistor layer is formed over or beneath the cathode, or ~~a~~ resistor layers ~~is~~ are formed both over and beneath the cathode in the FED.

Please replace the paragraph bridging Pages 3 and 4, with the following:

The present invention will now be described more fully with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. Referring to FIG. 2, which is a sectional view of a preferred embodiment of a field emission device (FED) according to the present invention. Referring to FIG. 2, a cathode 120 is formed over a substrate 100 with a metal such as chromium (Cr), and a resistor layer 130 is formed over the cathode 120 with an amorphous silicon. A gate insulation layer 140 with a well 140a, through which the bottom of the resistor layer 130 is exposed, is formed on the resistor layer 130 with an insulation material such as SiO_2. Use of the resistor layer 130 is optional. In other words, formation of the resistor layer 130 may be omitted so that the cathode 120 is exposed through the well 140a. Figs 2A and 2B

illustrate embodiments in which the resistor layer is above, and above and below, the cathode layer, respectively. A micro-tip 150, which is a feature of the present invention, is formed in the well 140a on the resist layer 130 with a metal such as molybdenum (Mo). A micro-tip 150 is a collection of a large number of nano-tips with nano-size surface features. The micro-tip 150 is formed of Mo, W, Si or diamond, or a combination of these materials.